Following is a listing of all claims in the present application, which listing supersedes all previously presented claims:

Listing of Claims:

Claims 1-12 (Canceled).

13. (Currently Amended) A semiconductor transistor, comprising:

a gate pattern formed on a semiconductor substrate;

an L-shaped ~~third~~ upper spacer having a horizontal protruding portion, the ~~third~~ upper spacer being formed on a sidewall surface of the gate pattern;

an L-shaped ~~fourth~~ lower spacer having a vertical sidewall between a vertical sidewall of the L-shaped ~~third~~ upper spacer and the gate pattern and a horizontal protruding portion between the horizontal protruding portion of the L-shaped ~~third~~ upper spacer and the substrate;

a high-concentration junction area formed to a first depth in the substrate beyond the L-shaped ~~third~~ upper spacer;

a low-concentration junction area formed to a third depth in the substrate under the horizontal protruding portion of the L-shaped ~~third~~ upper spacer, the first depth being greater than the third depth; and

a medium-concentration junction area formed to a second depth in the substrate and positioned between the high- and low-concentration junction areas and beyond the vertical sidewall portion of the L-shaped upper spacer, the second depth being between the first and third depths.

14. (Currently Amended) The semiconductor transistor as claimed in claim 13, wherein the medium- and low-concentration junction areas are formed under the horizontal

protruding portion of the L-shaped ~~third~~ upper spacer.

15. (Currently Amended) The semiconductor transistor as claimed in claim 13, wherein the L-shaped ~~fourth~~ lower spacer is made of silicon oxide.

16. (Currently Amended) The semiconductor transistor as claimed in claim 13, wherein the L-shaped ~~third~~ upper spacer is made of a material having an etch selectivity with respect to the L-shaped ~~fourth~~ lower spacer.

Claims 17-25 (Canceled).